TLP: ESD models correlation and aproximation

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***Abstract*— There are several models which try to describe the waveforms and damage produced by an electrostatic discharge event –ESD- to an integrated circuit –IC-, or more generally to a semiconductor device –SD-. The Transmission Line Pulse –TLP- test is widely used to run tests in this field, so it is needed to keep close correlation to the models used in different standards, in order to validate its results. This work analyzes the search of an approximate correlation, through tests, measurements and PSpice simulation, in order to predict, through the use of TLP information, the results of applying different standard ESD waveforms to a Device Under Test –DUT-.**

I. INTRODUCTION

Every integrated circuit -IC- or generally any semiconductor device -SD-, is vulnerable to an electrostatic discharge event -ESD-, where voltages and currents involved are very high, compared to the device's regular working conditions [1,2]. Furthermore, as SDs sizes shrink due to the constant evolution of fabrication technology, their susceptibility to ESD increases. The type of ESD events strongly depends on the elements that interact with the device, which could be circuits, humans and/or any kind of machinery. Different models exist to describe those different events, such as the human body model -HBM-, the machine model -MM-, the charged device model -CDM-, and so on [3,4,5,6,7,8,9,10]. A model widely used in the test field for analyzing the behavior of a SD when exposed to an ESD event, is the Transmission Line Pulse -TLP-. Though it differs from the models previously mentioned, it permits to extract useful information out of the SD [11]. Since ESD test results depend on the test model applied, standards such as IEC 61000-4-2 [5] or ANSI C63.16 [6], among others, can't bring coincident results to find a more general way and extend them to any waveform to be applied to a SD. Fig. 1 shows the different waveforms of the models mentioned.

Despite not being a standard, TLP is nowadays the preferred test method to run ESD tests on SDs. Then it is very important to know its features in order to correlate the test results to the different standard models [12,13,14].

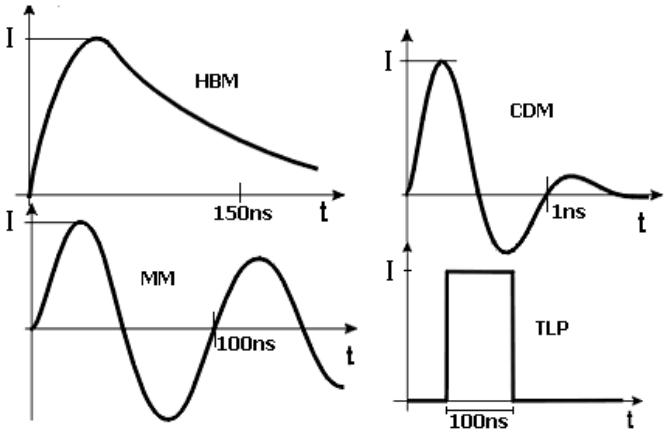

Figure 1. Waveforms of some ESD models

The method implements a square waveform with controlled amplitude and time length, which would not represent any of the mentioned ESD waveforms yet. But this method allows to apply a waveform with similar time length and specific energy to those present on the other ESD models. Even though, its a different signal and has its own frequency spectrum and characteristic times, which rise the main doubts when correlating its results with the different ESD models [15,16,17].

II. THE TLP

A. How it works

The TLP, which basic scheme is shown on Fig. 2, discharges a transmission line on the device, generating a square waveform. A high voltage source previously charges the line and then is discharged on the test device, getting a square current pulse on the device. The high voltage source V_G controls the waveform amplitude, while the pulse duration is set by the time delay determined by the transmission line length.

V_G charges the L_1 line through the R_G resistor, and the L_2 line connects the DUT to the circuit, whereas the attenuator absorbs reflected waveforms from the DUT.

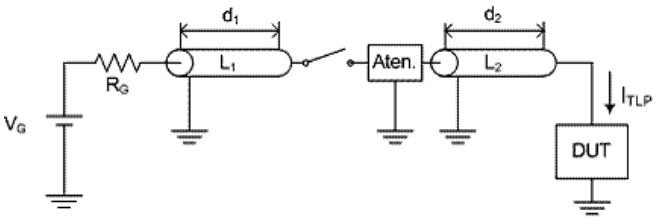

Figure 2. Basic TLP scheme

From the high voltage source to the DUT, the system has constant impedance which is the line's characteristic impedance, Z_0. Thus, all the components in the signal path has a characteristic impedance Z_0: lines L_1, L_2 and the attenuator [12,18]. The advantage of this system is that the pulse shape is not altered, mainly in it's rise-time, because it travels through an adapted system.

However, its rise-time is limited by the commutation speed of the system switch, and also by any losses present in the lines. It's worth mentioning that the switch is a key point due to the fast times involved in the event. TLPs generally use mercury-wetted reed relays, which can achieve the needed specifications, due to their fast switching time and a bounce-free contact.

B. Equipment used

The TLP equipment to be used is a TLP 50 model from TLP Solutions [19], which block-diagram is shown in Fig. 3. Fig. 4 shows, as an example, the I-V trace of a zener diode, using the TLP 50.

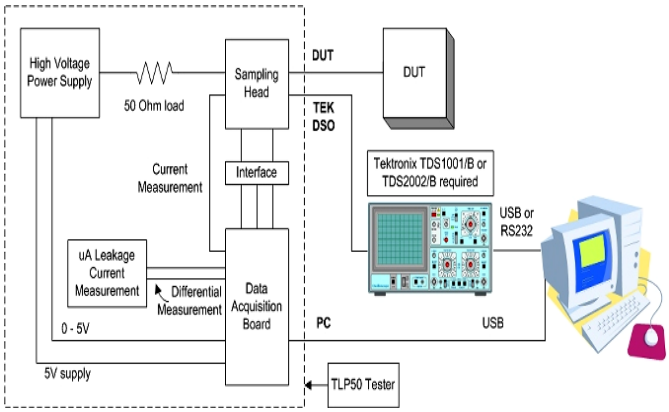

Figure 3. TLP50 block-diagram

III. MEASUREMENTS FOR 100NS AND 200NS PULSE WIDTHS

Even though several tests were run on different SD, such as zener diodes, discrete transistors, double gate MOSFETs, Hall-effect ICs, and so on; this work is focused on the results obtained from using a BS170 [20], a discrete MOSFET switching transistor, in order to avoid showing many results, but showing enough to make a basic analysis of the correlation found, which applies for the other SD tested as well.

Fig. 5 shows the I-V trace for a BS170, ran for 100ns pulses from 0 to 1kV. The snapback in the trace is very clear, and occurs for a pulse which had a V_G = 840V approximately, which causes the device to fail.

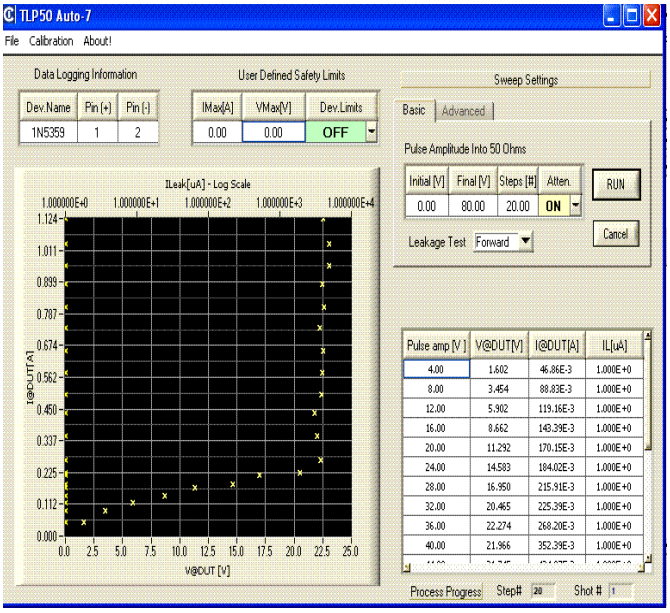

Figure 4. TLP50: Windows enviroment

Fig. 6 shows Vds(t), for some of the applied stepping up pulses. It can be seen that Vds is kept almost constant, somewhat higher than the breakdown voltage, until the snapback and failure point is reached. The trace marked with an arrow is where the snapback happens.

These traces were obtained for a statistic sample of transistors, where standard deviation among the traces was below 1%.

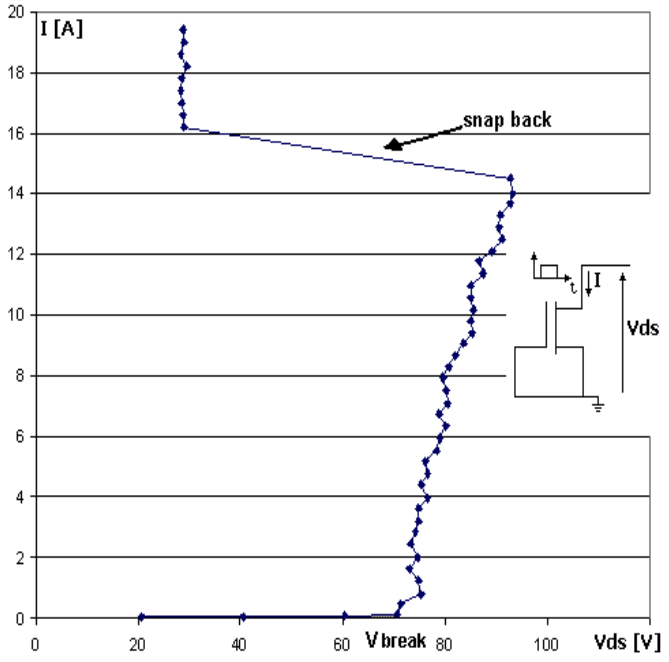

Figure 5. I – V trace for 100ns pulses

Based on these measurements, a new test was made: repetitive pulses of a voltage below the failure voltage on the I-V trace, was applied to the devices. The time between pulses was enough to keep the device at room temperature for each

pulse, so every pulse was applied in the same circumstances than the previous ones. The result of this test was a set of Vds vs time traces similar to those found on Fig. 6, but not having destroyed the device in any case.

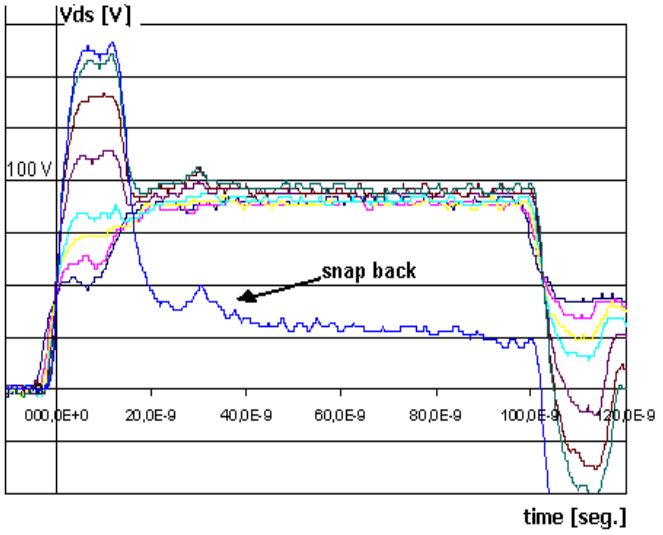

Figure 6. Vds (t) for 100ns growing pulses

Afterwards, and for a new statistic sample, a 200ns TLP pulse run was applied to find the I-V trace for that pulse width. For this test, the d_1 -Fig.2- was twice the original length. The traces were similar to those on Fig. 5. However, running the same repetitive pulses below the failure threshold didn't cause the device to fail for 100ns. Now, for 200ns the devices were destroyed in the first pulse in all the cases, showing Vds(t) waveforms similar to that on Fig. 7. Notice the device is destroyed at 40ns, which happens in the second 200ns pulse.

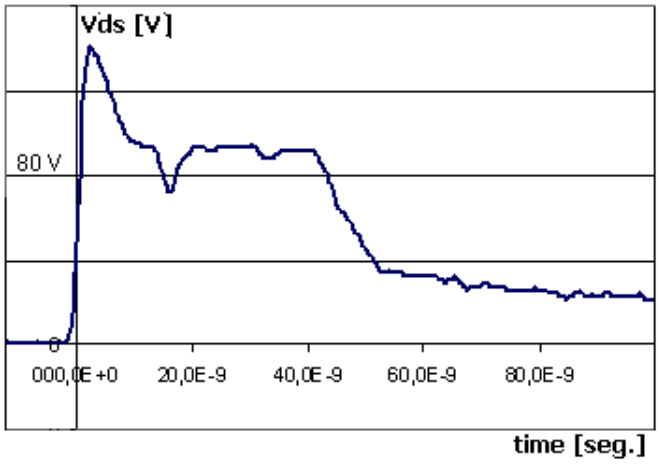

Figure 7. Vds(t) breakdown for 200ns pulse

Then, we used a HBM waveform model, modifying the TLP waveform, and testing again new samples of BS170. The snapback, with $V_G \leq 1$ kV, was reached increasing the width pulse, until almost three times the HBM standard fall time. This HBM waveform is shown on Fig. 8a. The snapback was reached at $V_G = 952V \pm 2.7\%$. Using MM waveform model, modifying again the TLP waveform –see Fig. 8b-, we never get the snapback point for $V_G \leq 1$ kV.

These results show that destruction could to happen due to over-heating stress, and thus for maximum absorbed energy. We will take it as our main parameter, in order to start estimating the correlation with different waveforms of other ESD events.

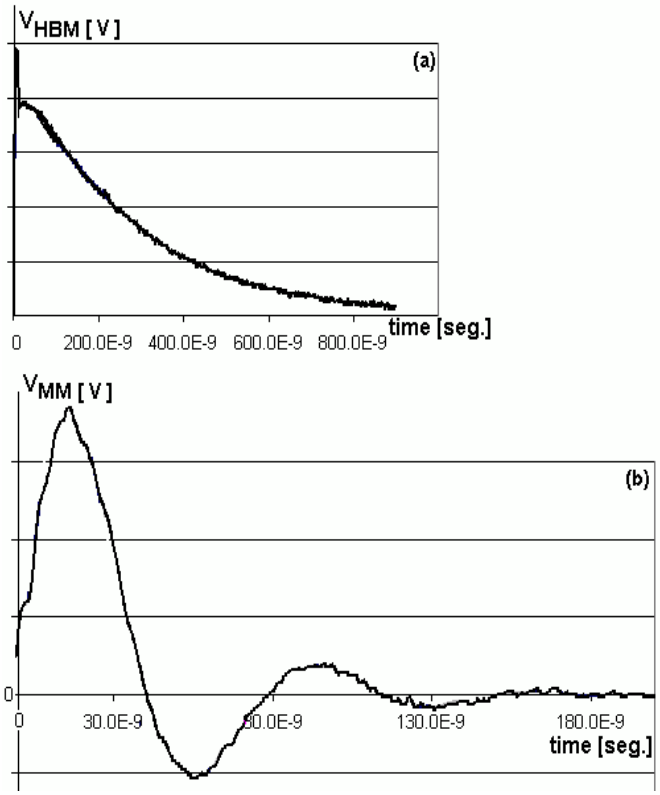

Figure 8. (a) HBM waveform modified. (b) MM waveform used.

IV. CORRELATION - APPROXIMATION

According to the results obtained in the tests, we start stating energy, or specific energy [Joule/Ω] as the parameter to correlate the different waveforms applied to the DUT. The method to follow is to adjust the V_G voltage according to the desired energy level to be transferred to the DUT. Specific energy transferred to the DUT for any waveform obeys (1):

$$E = \int_0^{\infty} {i_{DUT}}^2 \cdot dt \qquad (1)$$

Assuming lineal behavior of the TLP circuit that tests the DUT, the current i_{DUT} will be proportional to V_G, and so specific energy transferred to the DUT follows square relation with V_G. For example, taking the HBM model as reference, charge voltages should obey the following relationship:

$$V_{Geq} \cong \sqrt{\frac{E_{HBM}}{E_{model}}} \cdot V_{Gmodel} \qquad (2)$$

Where V_{Gmodel} and E_{model} are the charge voltage and the specific energy of the particular model, specified by its own standard; for this example, E_{HBM} is the HBM specific energy

and V_{Geq} is the charge voltage of the TLP that equals its specific energy to the HBM's.

From (2), charge voltage values V_{Geq} can be obtained for the different models. Those values are shown in Table I, whose reference model is the HBM. The table also shows the standard that defines every model.

TABLE I

Model/Standard	E_{model} [μJ/Ω]	V_{Gmodel} [kV]	$V_{Geq\ (E\ HBM)}$ [kV]
HBM / MIL-STD-883G	0.13	2	2
HM-HBM / ANSI C63.16	2.12	2	0.5
HBM 4° / MIL-STD-883G	0.1	2	2.3
MM / EIA/JESD22-A115-A	1.07	0.4	0.14
CDM / ESD STMS 3.1	0.02	0.5	1.3
TLP	0.4	1	0.58

The estimated correlation between models is shown on the fourth column of Table I. Even though this work was based on tests made with TLP, V_{Geq} values takes the HBM as the main reference, due to the fact that it's the historical ESD reference model.

The correlation found is obviously not the only one that could be analyzed. For example, the alternating polarity voltages in MM and CDM models could produce internal dynamic effects in each SD, and could not be fully correlated with energy. However the correlation due to over-heating stress, can build a simple model for predicting failure, for a first behavior approximation of the DUT.

An interesting relationship can be seen through solving equation (1) in the frequency domain.

$$E = \int_0^\infty I(\omega)^2 \cdot d\omega = I(0)^2 \cdot \int_0^\infty T(\omega)^2 \cdot d\omega \qquad (3)$$

Where I(0) ≡ Q, which is the initial charge of the particular ESD model to analyze, and T(ω) is the function that shapes the frequency spectrum of the discharge current of each model. Then:

$$E = Q^2 \cdot 2\pi \cdot f_E \qquad (4)$$

Where, the Frequency of same Energy level of each specific model is defined as in (5):

$$f_E = \frac{1}{2\pi} \cdot \int_0^\infty T(\omega)^2 \cdot d\omega \qquad (5)$$

A graphical interpretation of (4) is shown in Fig. 9, where can be seen that from the spectrum of $I(\omega)^2$, its specific energy can be obtained through f_E and I(0).

Graphically, the specific energy Er, which is obtained for a particular model, equals the area below the curve in Fig. 9, obtained through (3). Using (4), that energy can be calculated through the enclosed area by I(0), from f = 0 to f_E –Ei-. Since f_E is a constant for each model, it can be obtained through (4) using just a pair of I(0) and E values. Frequencies f_E of each model are shown in Table II.

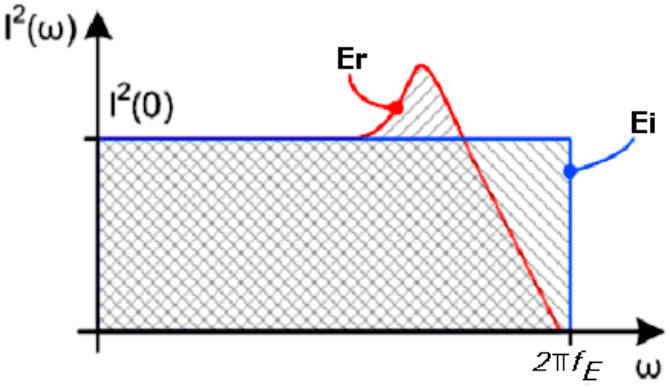

Figure 9. Graphical interpretation of equation (4)

TABLE II

Model	HBM	HM-HBM	HBM-4°	MM	CDM	TLP
f_E [MHz]	0.5	2	0.4	27	800	1.6

V. Simulation Model

To verify the results of the tests performed, the model depicted in Fig. 10 [21] was used to simulate the BS170 MOSFET in Orcad-PSpice [22]. This model was fine-tuned according to the measurements taken in the TLP tests. Even though are not shown in the figure, some large-value resistors were added in shunt to the model in order to avoid convergence problems that were present in some of the simulations.

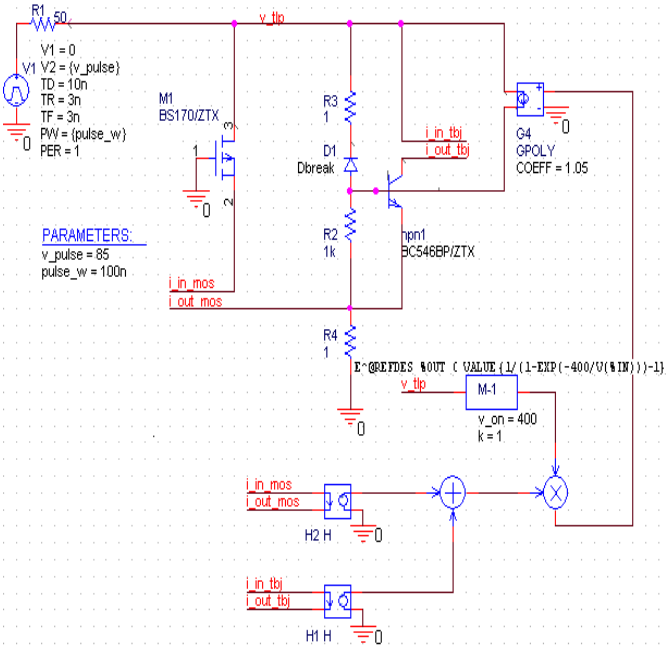

Figure 10. BS170 PSpice model

Vds(t) traces were very similar to those obtained in the TLP tests. The simulations helped to adjust V_G and f_E for each model, by applying each model's waveform, to obtain an approximate correlation between the models.

VI. CONCLUSION

The analysis to obtain an approximate correlation between different ESD models was focused on a semi-empirical analysis, based on TLP tests, which is a very common tool, and relying on Orcad-PSpice simulation. The SDs shown in this paper, as well as all the other devices tested, not shown in this work, keep similar relations and values, so it could be inferred that the estimation based on energy, is valid beyond the fabrication technology.

It emphasizes that energy could not the only the parameter to analyze a correlation. However, taking energy as an important correlation parameter enables a simple failure model that does not involve a detailed analysis of the internal behavior of the DUT and as a first approximation to predict their behavior due to an ESD event.

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